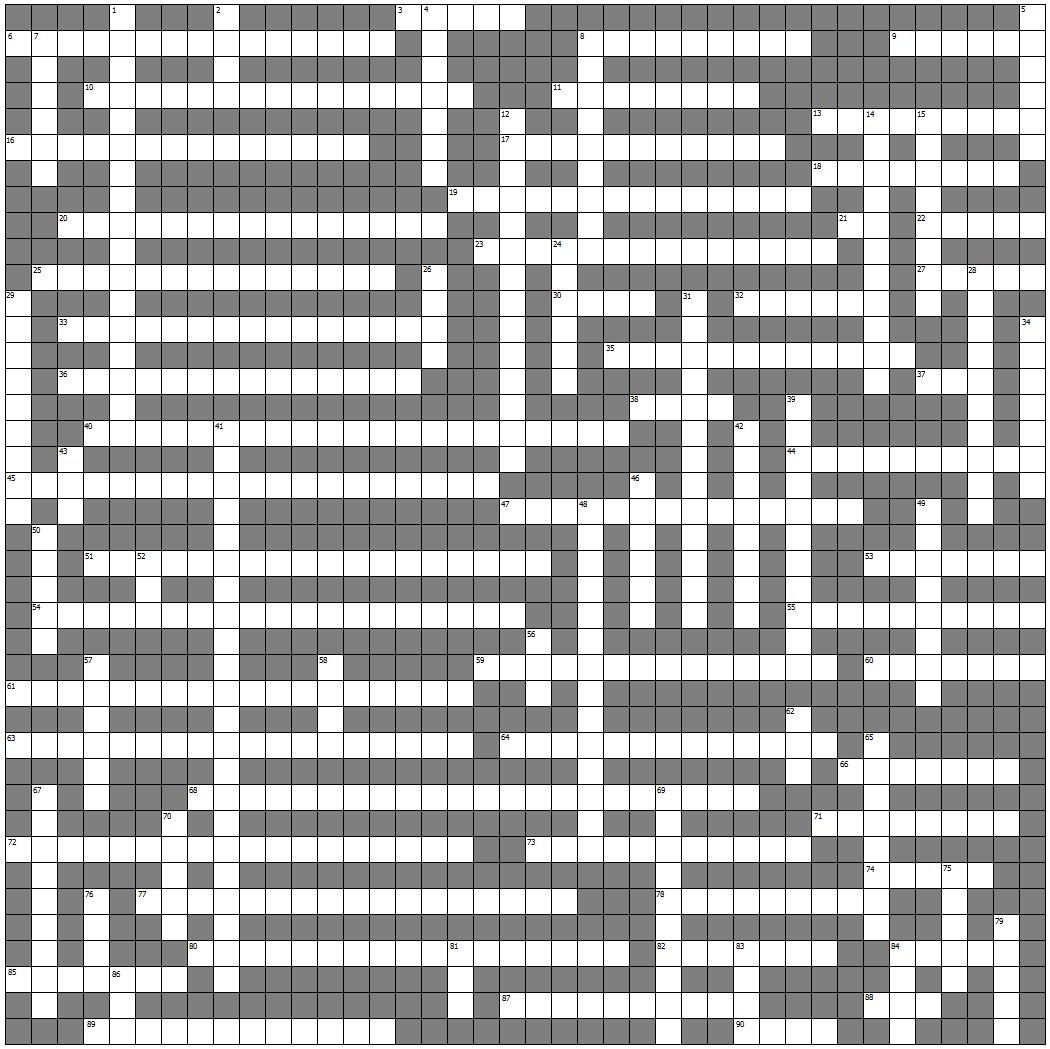
**Crossword**



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| --- | --- | --- | --- |
|  | Across: |  | Down: |
| 3. | 7 bit unsigned integer encoding for alphanumeric symbols. (5) | 1. | CPU operation. (5,7,5) |
| 6. | Dependent on present and prior input. (10, 5) | 2. | Logic gate. (4) |
| 8. | Algorithm or process representation. (4,5) | 4. | Cross coupled NORs. (1,1,5) |
| 9. | 4 bits. (6) | 5. | Electronic storage. (6) |
| 10. | Mammal in superposition. (12,3) | 7. | Type of memory. (6) |
| 11. | 1 bit memory circuit. (4,4) | 8. | One bit add with carry circuit. (4,5) |
| 13. | Program that translates symbolic instructions to binary. (9) | 12. | Designed difference engine. (7,7) |
| 16. | Calculus of truth. (7,7) | 14. | Computer Architecture. (11) |
| 17. | Base 16. | 15. | Floating point part. (8) |
| 18. | Index. (8) | 24. | Specifies operation. (6) |
| 19. | S=R=1. (9,5) | 26. | 2 Bytes (4) |
| 20. | Instructions and data executed directly by a CPU. (7,8) | 28. | Inventor of theoretical device that manipulates symbols contained on a strip of tape. (4,6) |
| 21. | Logic gate. (2) | 29. | Suspension of program execution to perform a higher priority service. (8) |
| 22. | Transfer data to. (5) | 31. | Number representation - fraction times a base raised to an integral power. (8,5) |
| 23. | Devices connected to address bus. (6,6,1,1) | 34. | Record of clock. (7) |
| 25. | Processor instructions. (11,3) | 39. | Two gated D latches in series. (6,5) |
| 27. | Last in, frst out structure. (5) | 41. | Performs integer arithmetic and logical operations. (10,3,5,4) |
| 30. | Low power architecture. (4) | 42. | Not. (8) |
| 32. | No match for Colossus. (6) | 43. | Binary digit. (3) |
| 33. | Computer on a chip. (15) | 46. | J=K=1 (6) |
| 35. | A + B = A . B ; A . B = A + B | 48. | CPU component. (6,8) |
| 36. | e.g. The Cell. | 49. | CPU memory. (8) |
| 37. | Logic gate. (3) | 50. | Study of reasoning. (5) |
| 38. | 8 bits. (4) | 52. | Logic gate. (3) |
| 40. | Computer executive. (7,10,4) | 56. | Logic gate. (3) |
| 44. | Section of code within a larger program. (10) | 57. | Base 2. (6) |
| 45. | Mechanical support for electronic components. (7,7,5) | 58. | Logical function circuit. (4) |
| 47. | Invert, add 1. (4,10) | 62. | Non volatile memory. (3) |
| 51. | Volatile memory. (6,6,6) | 65. | Program that translates a high level language to assembly language. (8) |
| 53. | Discrete system. (7) | 67. | Long term trend in computing hardware. (6,3) |
| 54. | CPU component. (11,8) | 69. | Tabular listing of logic combinations. (5,5) |
| 55. | CPU communication system. (7,3) | 70. | Integrated circuits material slice. (5) |
| 59. | CPU component. (7,7) | 75. | Periodic signal. (5) |
| 60. | Quantity on which an operation is performed. (7) | 76. | Information. (4) |
| 61. | e.g. Mealy / Moore. (6,5,7) | 79. | SI unit of frequency. (5) |
| 63. | Decimal coding system. (6,5,7) | 81. | Logic gate. (3) |
| 64. | Crystalline material doped by impurities. (13) | 83. | Architecture designed on a small number of primitive instructions. (4) |
| 66. | Interrogated one at a time. (7) | 84. | Colloquial name for an integrated circuit. (4) |
| 68. | Stored program architecture in which a single processor operates sequentially. (3,7,12) | 86. | Parallel conductors that carry information. (3) |
| 71. | Pre fetch architecture. (8) |  |  |
| 72. | Depends only on the inputs. (13,5) |  |  |
| 73. | Method to simplify Boolean algebra. (8,3) |  |  |
| 74. | Level triggered device. (5) |  |  |
| 77. | Gates with feedback. (10,7) |  |  |
| 78. | Sequence of signals exchanged by devices in preparation for data transfer. (9) |  |  |
| 80. | Symbolic language with strong abstraction from architecture. (4,5,8) |  |  |
| 82. | Location data. (7) |  |  |
| 84. | Fast memory that holds recently accessed instructions or data. (5) |  |  |
| 85. | CPU communication System. (4,3) |  |  |
| 87. | CPU communication System. (7,3) |  |  |
| 88. | Result of dicing. (3) |  |  |
| 89. | Not clocked; often controlled by handshaking. (12) |  |  |
| 90. | Architecture in which each instruction can execute several low level operations. (4) |  |  |